Comparison of Ion Implantation Approaches in the Fabrication of AlGaN/GaN HFETs: Classical *vs.* Through the Gate Metal

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Ion implantation isolation is well-suited to the fabrication of AlGaN/GaN heterostructure field-effect transistors (HFETs) because of the large energy gaps in III-N materials. The use of ion implantation maintains a planar surface topology and facilitates the high-yield implementation of narrow gate fingers. Unfortunately, the high implant doses can harden photoresist masks and necessitate thorough wafer cleaning prior to the gate lithography step.

In the present work, we demonstrate transistor fabrication process architecture with the ion implantation isolation carried out *through the gate metal* and compare device performance to that of devices fabricated following the conventional process flow wherein the isolation implantation is carried out prior to the gate metallization. Implantation through the gate metal is advantageous because the transistor active region is never exposed to hardbaked/polymerized photoresists nor to harsh resist removal treatments, ensuring a pristine metal/semiconductor Schottky contact.

AlGaN/GaN HFETs of various gatelengths were implemented on MBE-grown AlGaN/GaN layers with a high-resistivity C-doped buffer deposited on sapphire substrates featuring electron densities of 10^{13} cm^{-2} and μ = 1,000 cm^2/Vs. Device fabrication started with the formation of Ti/Al/Ti/Al (400 / 800 / 300 / 800 Å) Ohmic contacts RTA annealed at 850°C for 30 s. The wafer was then cleaved and one half continued to implant isolation while the other half immediately proceeded to gate lithography. In both samples, implant isolation was carried by P/He with doses and energies selected based on SRIM simulations. Both process splits featured isolation sheet resistances ranging from 30 - 40 GΩ/square. In both cases, the shielded active areas retained the pre-implantation sheet resistance of ~ 650 Ω/square as measured by TLM pattern measurements.

Long gate transistors with L_G = 10 μm as well as submicrometer devices were successfully implemented. The long gate devices were first studied to better characterize the effects of ion implantation isolation. Devices isolated through the gate metal displayed higher peak transconductances, lower gate leakage currents, and a less negative pinch-off voltage. The results indicate that performing the gate metallization prior to the implantation isolation results in a cleaner metal/semiconductor interface. Microwave devices isolated through the gate metal revealed peak f_T = 18 GHz for a 0.4 μm gate length confirming the efficacy of this new process architecture. Our presentation will discuss the details of the fabrication process, and provide a full discussion of the impact of the ion implantation isolation approach on the the DC/RF device characteristics of the devices.

This work was supported by NSERC and *Nortel Networks*.

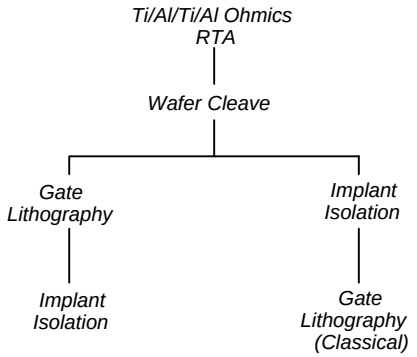

Figure 1: Process splits implemented in the present experiments.

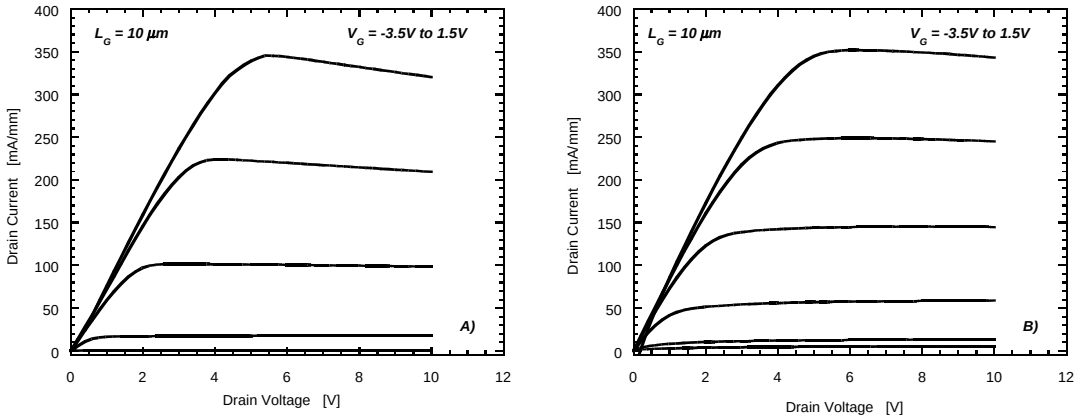

Figure 2: a) Implant isolation <u>after</u> gate metallization; b) Implant isolation <u>before</u> gate metallization. In both cases the gate voltage step is 1V. Note that devices implanted after gate metallization clearly feature a higher transconductance.

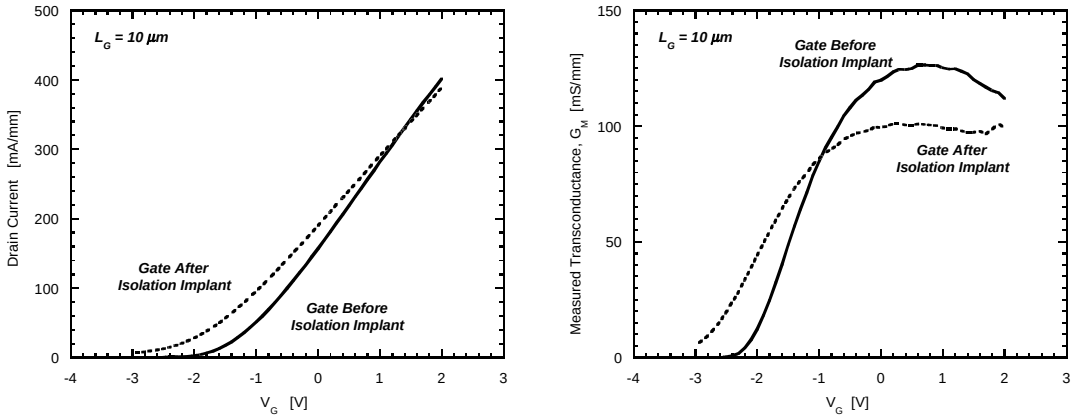

Figure 3: Dependence of I_{DS} and of transconductance on the implant isolation process.